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Improved Power Modeling of DDR SDRAMs

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Outline

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- SDRAM Basics
- Problem Statement
- Existing Power Models - What's missing?
- Where do we stand?
- Our Approach
- How do we do it? - Generic Power Model
- How do we compare? - Power and Energy Estimation
- Are we there yet?
- Conclusions

Why?

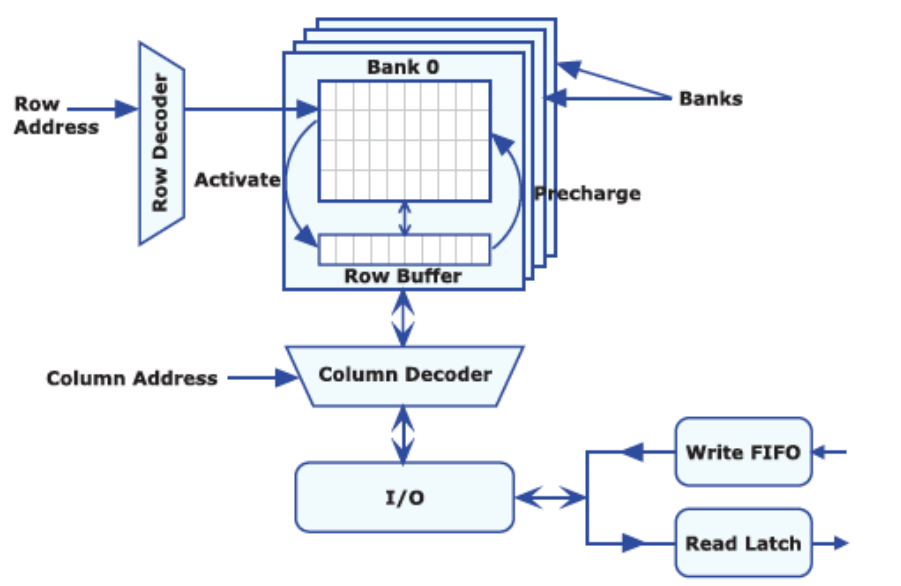
- DDRs contribute significantly to total system power
  - As high as app. processors in smart phones - Infineon*
  - “Memory will be the largest power consumer in servers in the years to come” - Intel Labs**
- Power modeling and estimation can be useful in:
  - Formulating scheduling policies in memory controllers
  - Identifying power/performance trade-offs
  - Defining SDRAM power management policies

*** Vargas, “Achieve minimum power consumption in mobile memory subsystems”, 2006**

**** Minas and Ellison, “The Problem of Power Consumption in Servers”, 2009**

DDR SDRAMs

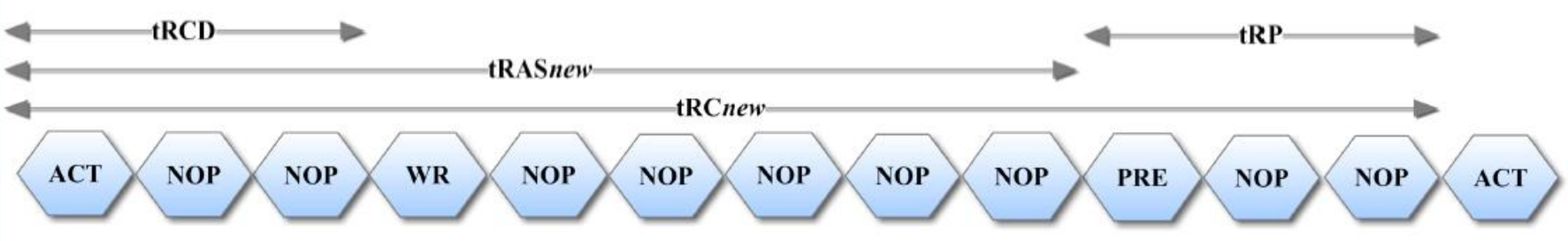
SDRAM Basics (1/2)



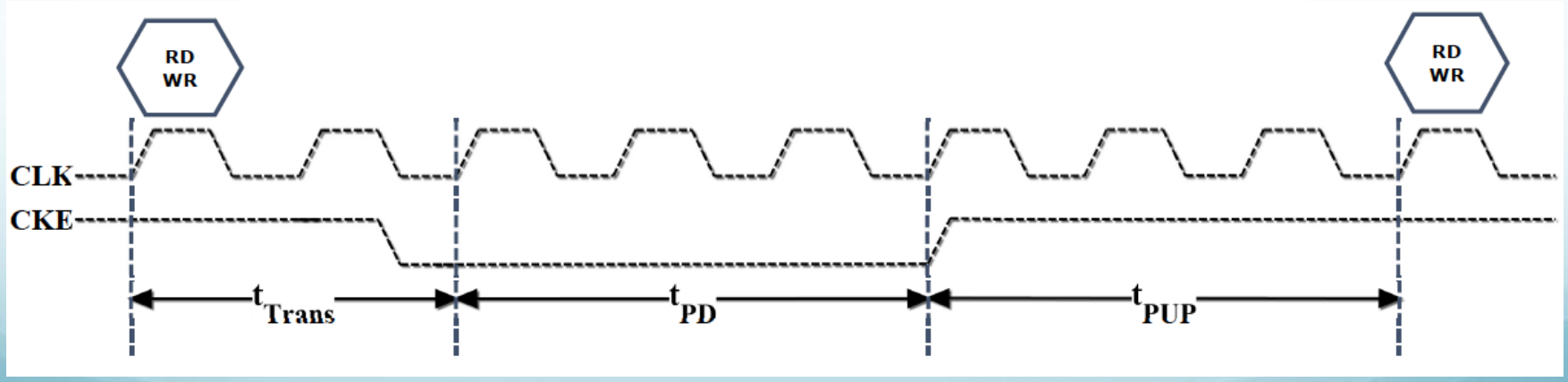
- Organized in Banks, Rows, Columns and Row Buffer
- Activate, (auto)Precharge, Read, Write, Refresh & Self-refresh
- Open/Close Page Policy (locality based) & Power-down

SDRAM Basics (2/2)

Timing Constraints (Minimum constraints vs. Actual Measures)



Power-Down State Transitions (JEDEC specs)



Problem Statement

To derive an accurate DDRx SDRAM power model that:

- Employs actual timings from a memory controller
- Accounts for memory state transitions accurately
- Respects JEDEC timing constraints
- Supports all page policies and memory access scheduling
- Is available and easily applicable for all users

Knock Knock, Who’s There?

Existing Power Models

- Based on SDRAM Datasheets using measured current and voltage values
  - Micron's Model (2004) - Most popular
  - Rawson's Model (IBM)
- Based on energy coefficients with an SDRAM energy state machine
  - Joo's Model (Seoul National University - DAC 2002)
- Based on device-level SDRAM details and technology specifications using switching activity
  - Rambus' Model (2010)

What's missing?

- Micron's and Rawson's Models
  - Use minimum timing constraints from SDRAM datasheets
  - Need for accurate scaling of active/background components
  - Supports Close-page policy by default- Pessimistic on power
  - Do not include transition periods to power saving states as power overhead - Optimistic on savings
- Joo's Model
  - Useful for designing memory systems
  - Abstract and cannot be used with a memory controller
- Rambus' Model
  - Device details are available only with memory vendors

Where do we stand?

Our Power Model & Micron's Power Model

- Both models employ measured current and voltage numbers from SDRAM datasheets
- Both models employ similar classification of basic power components such as read, write, background power

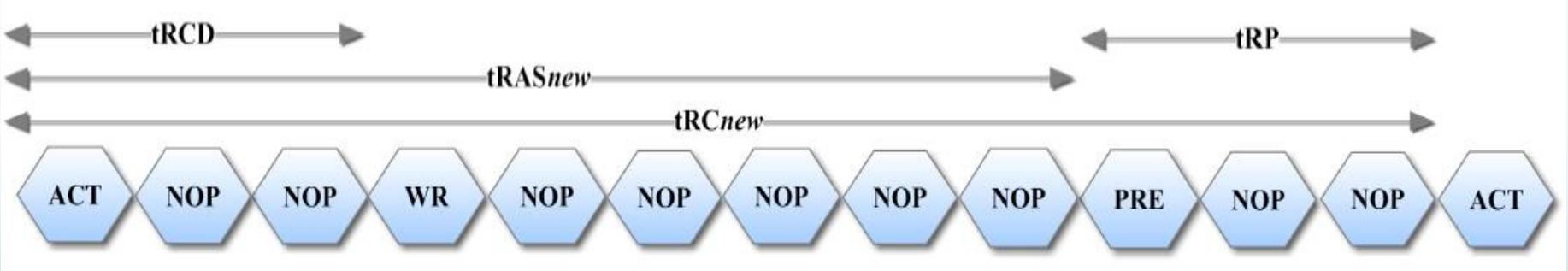
Our Power Model Vs. Micron's Power Model

- **Actual timing measures** Vs. Minimum timing constraints
- **Includes state transitions as overhead** Vs. No so!
- **Supports Open and Close-page policy** Vs. Close-page only

Our Fix!

Our Approach (1/2)

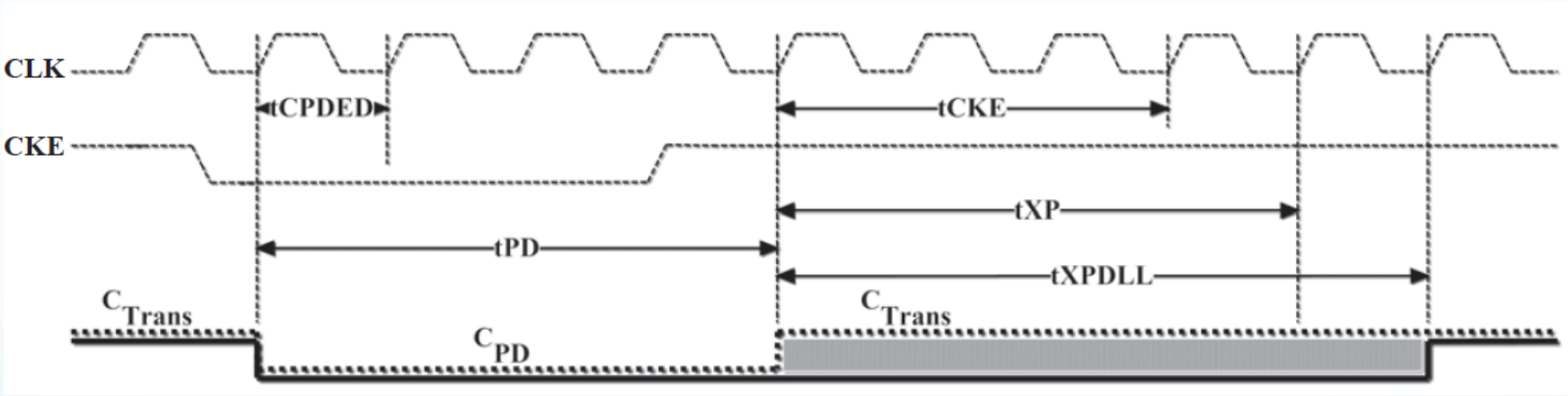
- Gets actual timing measures from an SDRAM command trace - ‘modified’ equations
- Supports open and close page policies - ‘new’ equations
- Uses cycle-accurate information



- Micron’s estimates are pessimistic (w/o scaling)

Our Approach (2/2)

- Takes into account all state transitions to all power-down states and refresh & self-refresh - ‘new’ equations



- Respects all min transition timings - minimizes overhead
- Micron’s estimates are optimistic (energy difference)

How do we do it?

Power Model - Timing Accuracy

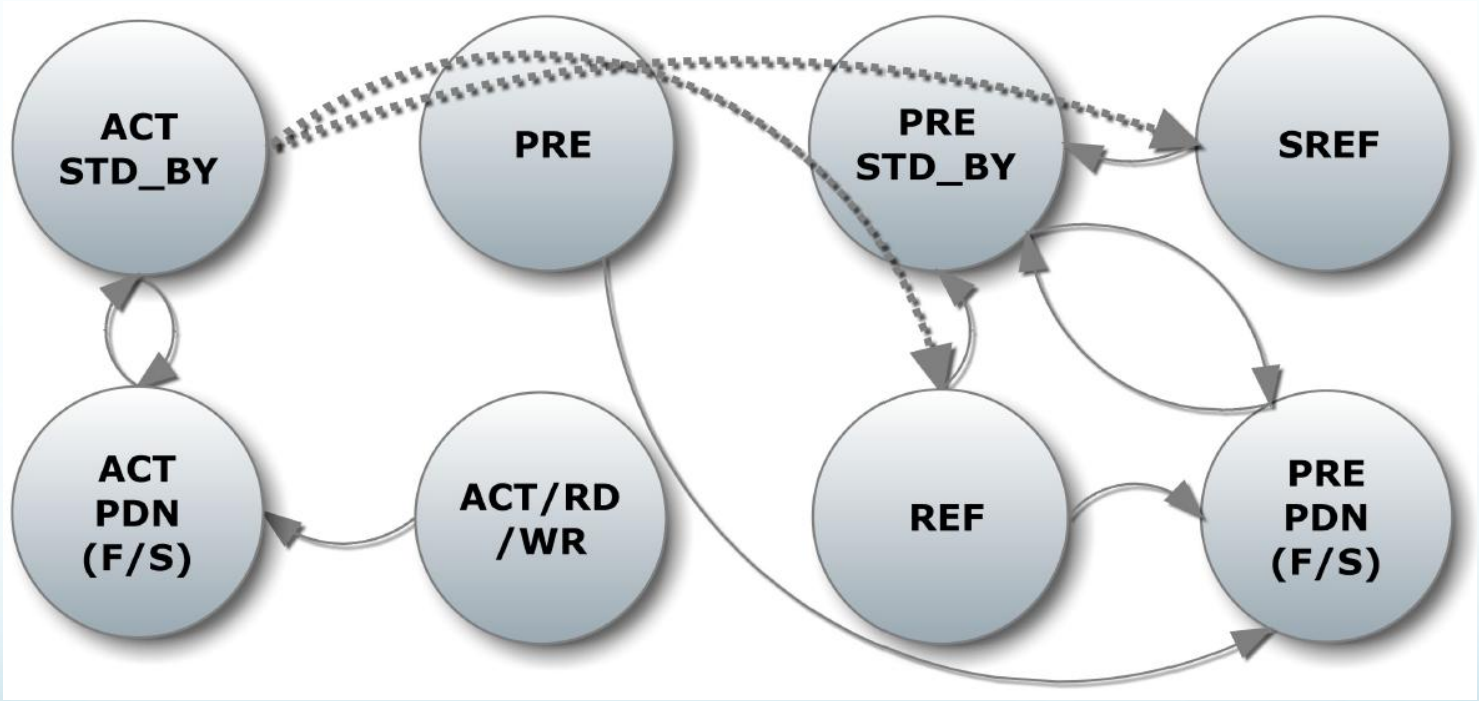
- Basic Power Components - Active and Background
- Cycle-accurate timing information used (with scaling)
- Active Components scale down and Background ones scale up

Command	ACT	NOP	NOP	RD	NOP	NOP	NOP	NOP	PRE	NOP	NOP
$P(ACT_{BG})$	X	X	X	X	X	X	X	X			
$P(PRE_{BG})$									X	X	X
P(ACT)	X	X	X	X	X	X	X	X			
P(PRE)									X	X	X
P(RD)					X	X	X	X			

* Not included: Refresh, I/O and Termination Power

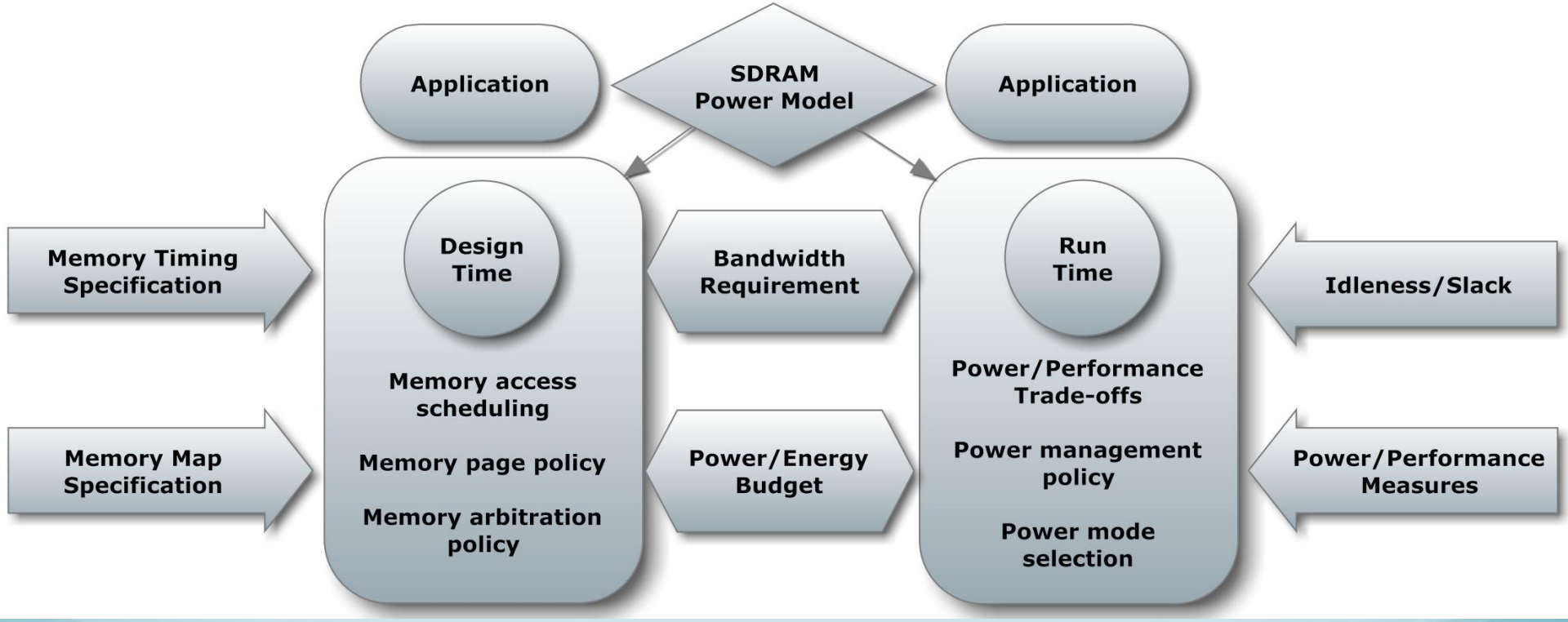
Power Model - State Transitions

All transitions to power-saving states and refresh are modeled



Controller Design-Flow Context

Granularity of analysis - from a transaction to an application



The Complete Picture

- Cycle-accurate analysis of each memory bank
- Open and Close-page policy supported
- Accurate (not minimal) timing measures employed
- All state transitions accounted for as overhead
- Easy integration with any memory controller setup

Plug n Play or Do it yourself?

How much did we improve?

Comparison - Basic Operations

Using accurate timings and support for open page policy

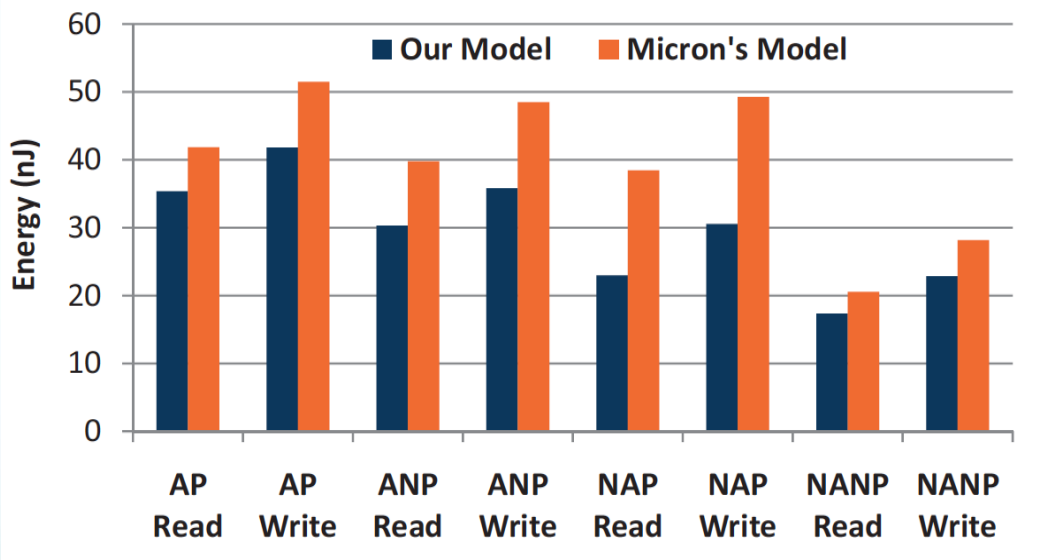
For DDR3-800 (128 bytes transactions)

AP : ACT - PRE

ANP : ACT - No PRE

NAP : No ACT - PRE

NANP : No ACT - No PRE

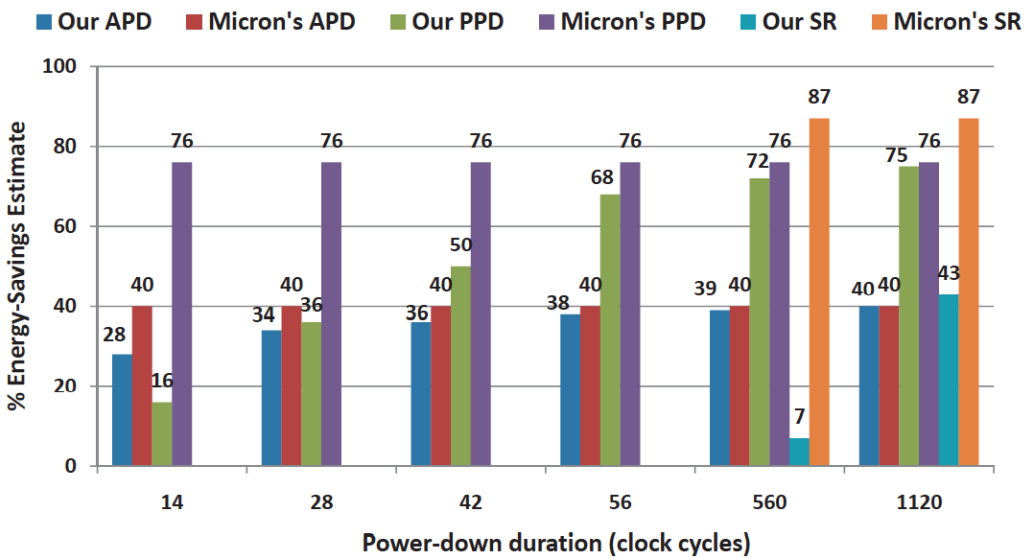


- ANP and NAP (Open page) - Activate-Precharge energy correction

Comparison - Power-Savers

Using all transitions to power-saving and Self-refresh modes

- APD - Act Power-down
- PPD - Pre Power-down
- SR - Self-Refresh
- 14 cycles - minimum PPD
- Compared to Stand-by energy



- State Transitions - overhead of switching to power-saving modes
- Lower granularity for operation - higher influence of transitions

Are we there yet?

- Schmidt and Wehn, “DRAM power management and energy consumption: a critical assessment”, SBCCI ’09
  - Showed that Micron’s model over-estimated power savings for SREF and provided worst-case estimates for regular operations
  - Our results in line with expectations - timings and transitions
- Preliminary verifications with circuit level power estimation (similar to Rambus)
- Extending to LPDDRs
- DDRx SDRAM Power and Energy estimation Tool (Open source) on its way!

Conclusions

- Our proposed DDR SDRAM power model is applicable to all memory controllers (real-time and non-real-time) and supports all scheduling and open-close page policies.
- Our power model provides accurate equations to cover all possible state transitions to power-down and self-refresh modes.
- We observe significant improvements in power and energy estimates over Micron’s power model.
- The soon-to-be open source tool will estimate and optimize memory power consumption for all DDRs.

Thank you!

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