

Towards Variation-Aware System-Level Power Estimation of DRAMs: An Empirical Approach

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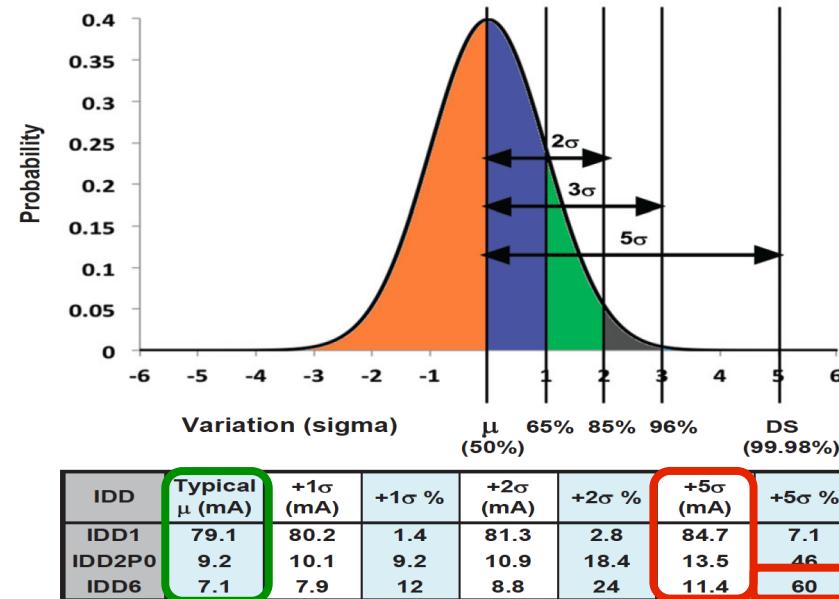
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Problem Statement

- Below 90nm, impact of process-variations on power is significant.
- Studied well for processors but NOT for DRAMs (worst-case IDDs).
- Unfortunately, this cannot be ignored! DRAMs influence system power.
- How severe is the impact of variations on DRAM power?



* Normal Distribution (μ, σ) for 11,000 DDR3 1Gb-533-x8 devices at 70nm

- Unfortunately, there are NO known models or measures publicly available.

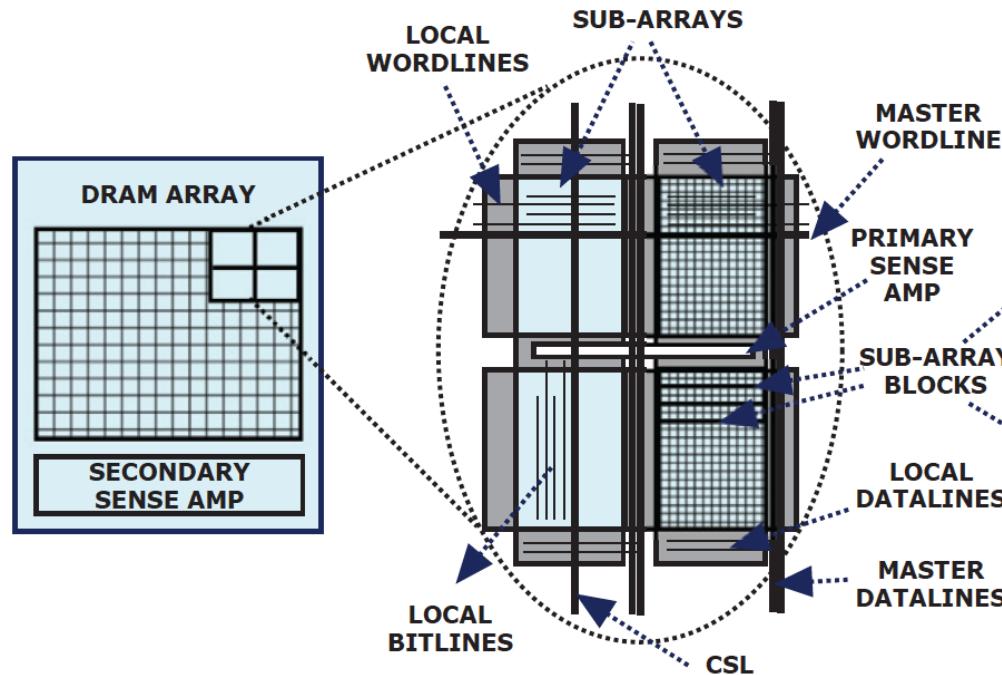
Contributions [What do we propose?]

- (1) To empirically estimate the impact of variation on DRAM power
 - Using Monte-Carlo simulations on a baseline SPICE DRAM cross-section.
 - Extending for different DRAM frequencies, capacities and data-widths.
- (2) To empirically characterize a given DRAM at boot-time
 - By assessing the actual performance of a given DRAM (dictates power).
- (3) To derive actual power consumption
 - Using distributions from the Monte-Carlo simulations.
 - Using the actual performance from characterization.

Estimation of impact of variation on DRAM power consumption

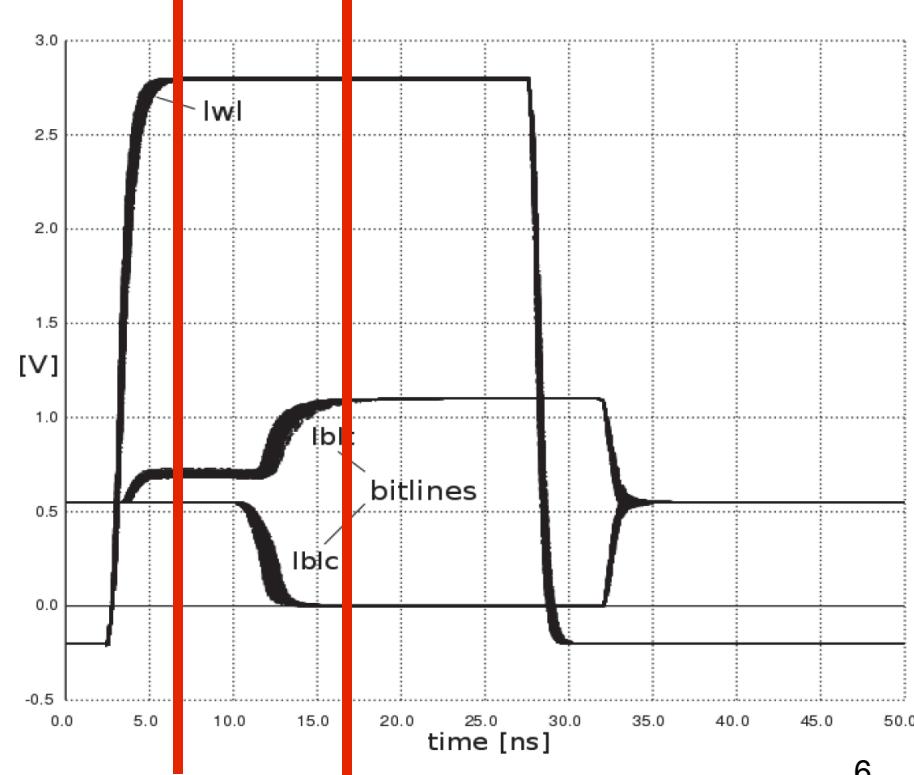
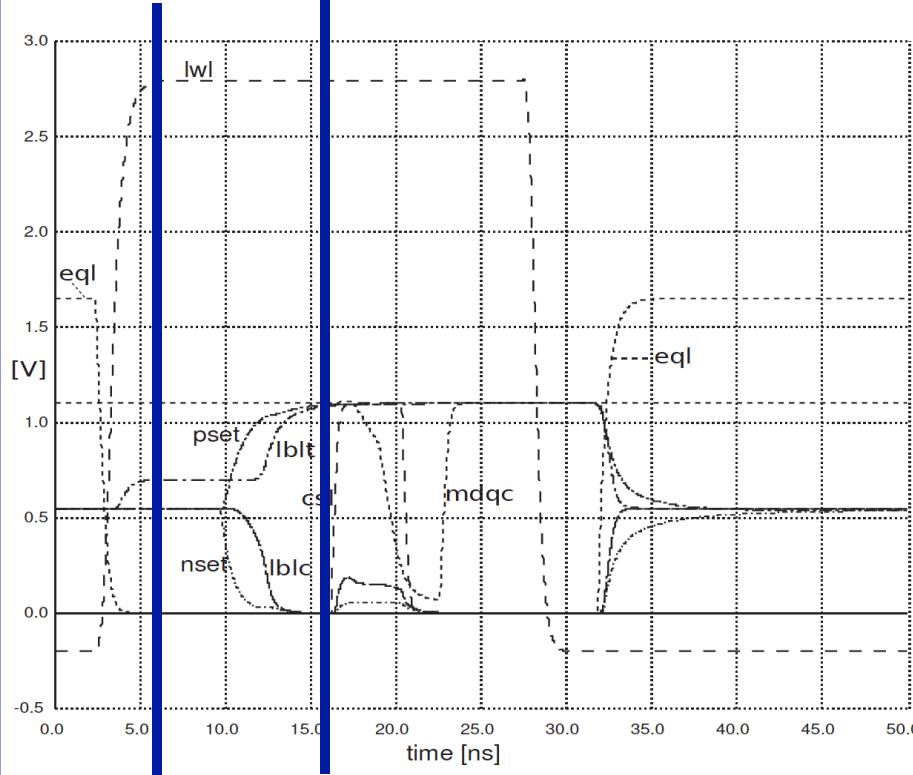
DRAM Cross-Section Modeling (SPICE)

- Baseline DRAM Bank cross-section model
 - NGSPICE - BSIM Model Cards - 45nm LP-PTM (Bulk CMOS)
 - 1Gb DDR3-533MHz - x8 data-width
 - Core Timings adhered to: CL-RCD-RP : 7-7-7 cc (JEDEC specified)
 - 1T1C DRAM cell & 512 cells per local bitline/wordline
 - Column Select Lines (CSLs) & Master Wordlines
 - Primary & Secondary Sense Amplifiers & IO Buffers



SPICE Simulation Results

- Functionality and Timings Verified: ACT-RD-PRE & Core-Timings
- Monte-Carlo: Device & Interconnect variations (ITRS/IBM) introduced
- 1000 MC runs in NGSPICE: 4 important device parameters
 - Global - Channel Length (l), Mobility (μ), Oxide Thickness (T_{ox}) & Local - V_{TH} (LER)



Impact of Variation on Currents (IDDs)

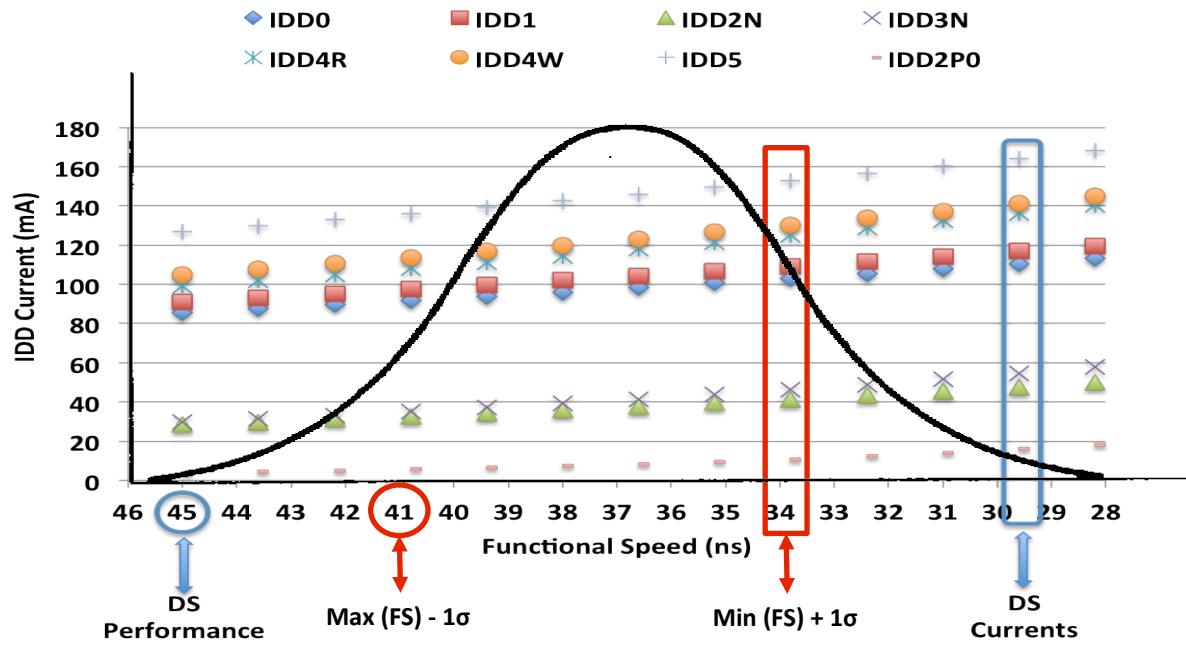
- Baseline, Monte-Carlo & Extensions: 3 parameters (Freq, Cap, Width)
 - Frequency [F] (533 to 800): All currents change except leakage
 - Capacity [C] (1Gb to 2Gb): Changes in all currents
 - Data-Width [W] (x8 to x16): Data transfer currents change

	Baseline		Freq		Capacity	
Config	1Gb-533-x8		1Gb-800-x8		2Gb-533-x8	
Type	μ mA	σ %	μ mA	σ %	μ mA	σ %
I_{DD0}	98.4	2.4	112	2.6	99.3	2.5
I_{DD1}	104	2.3	118	2.2	105	2.5
I_{DD2N}	37.7	4.8	42.7	4.5	46.5	6.1
I_{DD3N}	41.5	5.7	56.7	4.5	49.9	5.3
I_{DD4R}	118	2.9	153	3.5	127	3.3
I_{DD4W}	123	2.7	159	4.1	132	3.7
I_{DD5}	146	2.1	161	2.4	184	2.2
I_{DD2P0}	8.4	13.7	8.4	13.7	16.6	16.1
I_{DD6}	8	14	8	14	13.7	19.9

Characterization of a given DRAM at boot-time

Characterization of a given DRAM at boot-time

- To identify actual performance and thereby, power of a given DRAM.
- Performance defined by: Core-timings & frequency- Functional Speed (FS)
- Get IDD & FS values for μ and $\pm 6\sigma$ variations (distribution) from SPICE.

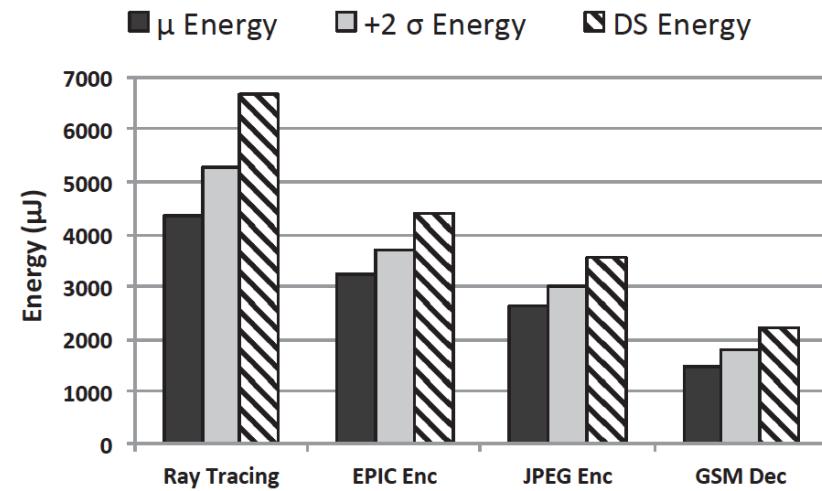


- @Boot-time, for all CT, F & banks, run IDD1 test: get FS/bank (< 100ms)
- Use $\text{Min}(\text{FS})$ of all - Fastest for IDDs ($+1\sigma$ conservative) - actual worst-case
- Optionally, Use $\text{Max}(\text{FS})$ of all - Slowest for CT & F (-1σ conservative)

Results & Analysis

- Mean Vs. Datasheet (DS): Micron 2Gb DDR3-800-x16 device (50nm)
 - Combining influence of all three system parameters (F, C & W)
 - μ is 30% < DS for active & 86% < DS for leakage (60% @ 70nm)
- Application energy differences:
 - 4 MediaBench applications: Ray Tracing, EPIC, JPEG Enc. & GSM Dec.
 - Up to 58% worst-case diff. using μ and 28% using $+2\sigma$

Current	DS mA	μ (mA)	μ vs DS %	2σ mA	2σ vs DS %
IDD0	110	98	-12.2	102.8	-6.96
IDD1	125	112.2	-11.4	117.3	-6.53
IDD2N	42	33.5	-25.4	36.9	-13.8
IDD3N	45	34.6	-30.1	38.7	-16.1
IDD4R	270	232.2	-16.2	247.3	-9.15
IDD4W	280	246.7	-13.5	260	-7.67
IDD5	215	193.6	-11.1	202.1	-6.34
IDD2P0	12	6.62	-81.1	8.77	-36.7
IDD6	12	6.45	-85.9	8.67	-38.4



Conclusions

Problems:

- Process-variations significantly impact DRAM power consumption.
- Vendors only provide worst-case current measures.
- Every DRAM device has individual performance and current measures

Solutions:

- We proposed variation-aware power estimation for DRAMs.
- We proposed boot-time DRAM characterization methodology.
- We identified actual DRAM performance and realistic power measures.
- Added new variation-aware datasheets to the open-source DRAM power tool - **DRAMPower**. Available at: www.drampower.info

Thank You!

Questions?

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www.drampower.info